SICC®

Product Catalog

山东天岳先进科技股份有限公司

SICC Co.,Ltd

Technology
Quality
Sustainable

COMPANY PROFILE

Technology | Quality | Sustainable

SICC is one of the leading SiC Substrates Manufacturing Company. It is established in 2010 in Jinan, Shandong, China. There are two types of main products, Semi-insulting substrates and N-type substrates, and two production plants in Shandong and a third plant in Shanghai.

SICC has rich experience in production & industrial development, and strong R&D capabilities. We focus on high-quality and multi-dimensional product development. Based on the market demand, we continuously improve our product quality. At the same time, we keep expanding the product portfolio to meet the needs of SiC substrates in more fields, including N-type substrate for power devices, semi-insulating substrate for micro-wave communication, and optoelectronic substrate for lighting, etc.

n-Type Substrates
Power device

Semi-Insulating Substrates
RF device

Photoelectric Substrates
LED

MF Substrates
Low and medium frequency/power device

Heat Sink Substrates
Heat sinking

Special-shaped Substrates
Optical purposes

Gemstone
Jewelry (Moissanite Diamond)

ISO9001 · ISO14001 · ISO45001 Certified

ISO9001

ISO45001

ISO14001

IATF 16949

IATF16949 is under certification

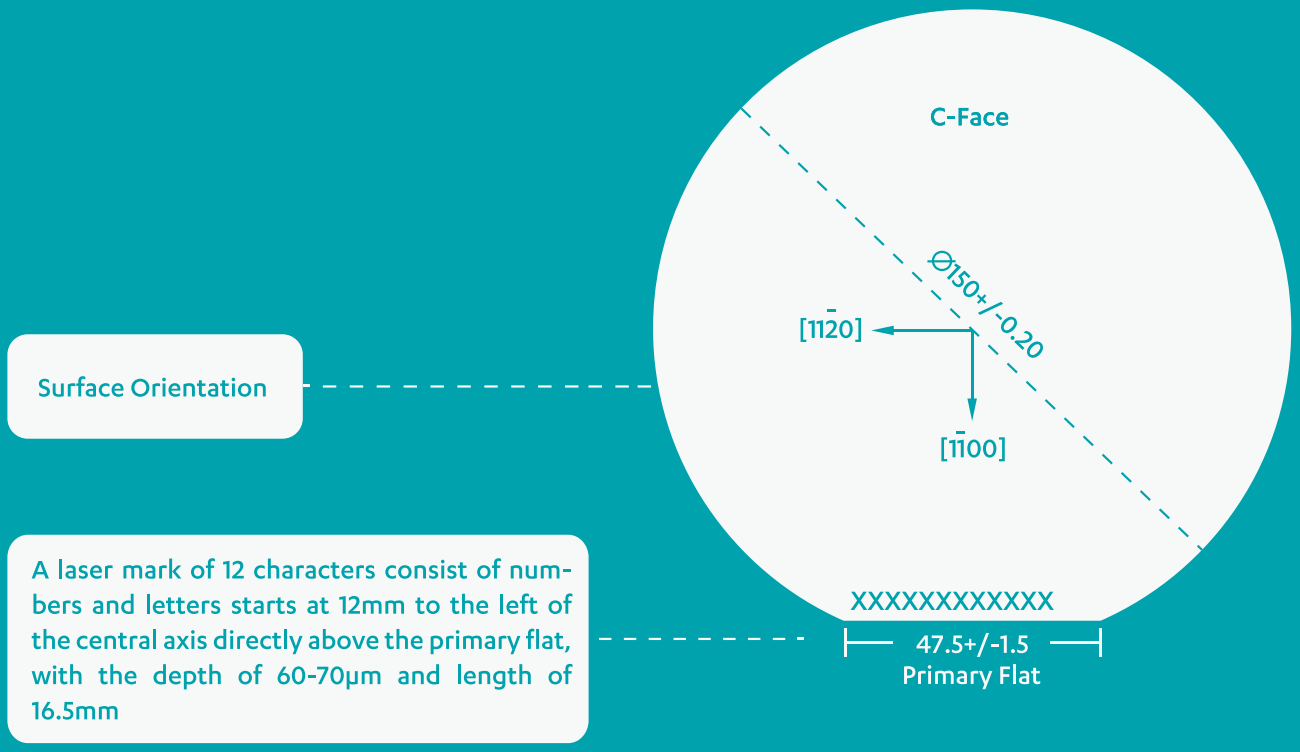
n-Type SiC SUBSTRATE
BASIC PRODUCT SPECIFICATION

Diameter[1]	150±0.2mm
Surface Orientation[1]	off-axis: 4°toward [11$\bar{2}$0] ± 0.5°
Primary Flat Length[1]	47.5 ±1.5 mm
Primary Flat Orientation[1]	[11$\bar{2}$0] ± 5.0°
Secondary Flat	None
Thickness	350.0±25.0μm
Polytype	4H
Conductive Type	n-Type

PROPERTIES, TERMINOLOGY, AND METHODS

01 Diameter /Primary Flat/Laser-mark information shown as Figure 1

Figure 1



n-Type SiC SUBSTRATE

CRYSTAL QUALITY SPECIFICATIONS

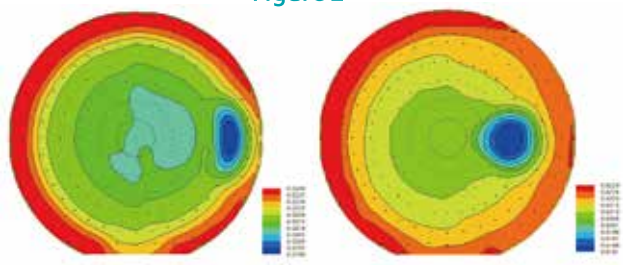
Item	Pm-Grade	Ps-Grade
Resistivity	0.015-0.025Ω·cm	
Polytype	None permitted	
Micropipe Density	≤0.2/cm²	≤0.5/cm²
EPD	≤4000/cm²	≤8000/cm²
TED	≤3000/cm²	≤6000/cm²
BPD	≤1000/cm²	≤2000/cm²
TSD	≤600/cm²	≤1000/cm²
SF （Measured by UV-PL-355nm）	≤0.5% area	≤1% area
Hex plates by high intensity light	None permitted	
Visual Carbon Inclusions by high intensity light	Cumulative area≤0.05%	

PROPERTIES, TERMINOLOGY, AND METHODS

01 Resistivity

Tested by Non-contact sheet resistance multi-points measurement system with eddy-current gauge

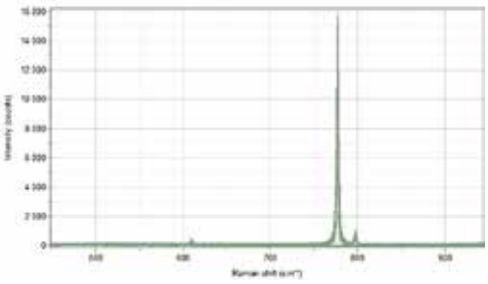
Figure 2



02 Polytype

Tested by Raman Spectrometers shown as Figure3

Figure 3



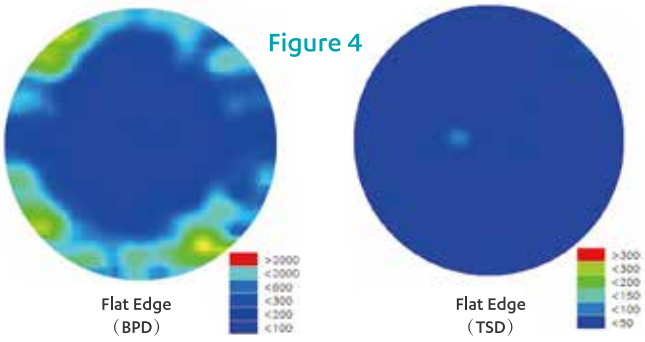
03 Micropipe density

Every substrate is tested by Surface scanning

04 BPD&TSD

One piece of substrate from each crystal is selected for KOH test shown as Figure 4

Figure 4



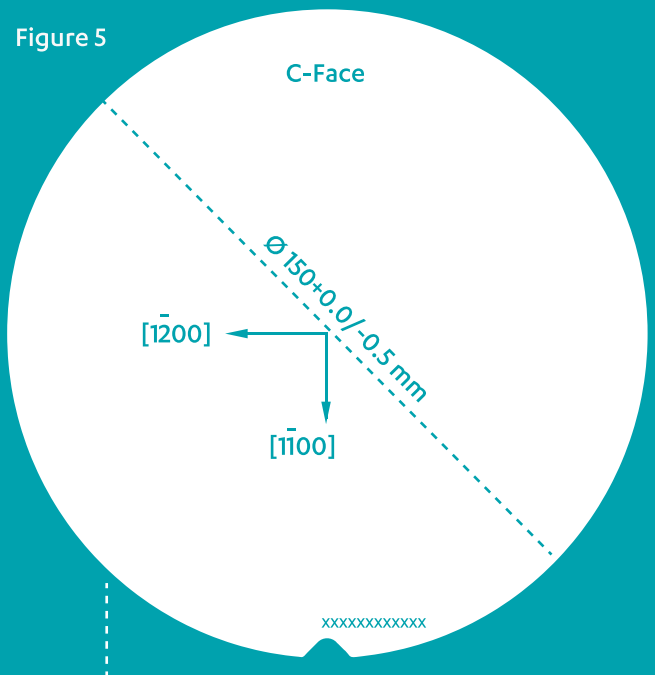
Semi-insulating SiC Substrate
BASIC PRODUCT SPECIFICATION

Diameter		100.0/150.0mm+0.0/-0.5 mm	
Surface Orientation		{0001}±0.2°	
Flat	4Inch	Primary Flat Orientation	[11$\bar{2}$0] ± 5°
		Secondary Flat Orientation	Silicon face up: 90° CW from Prime flat ±5.0°
		Primary Flat Length	32.5 mm ± 2.0 mm
		Secondary Flat Length	18.0 mm ± 2.0 mm
	6Inch	Notch Orientation	[1$\bar{1}$00] ± 1.0 °
		Notch Depth	1.0 mm +0.25 mm-0.00 mm
		Notch Angle	90°+5°/-1°
Thickness		500.0μm± 25.0μm	
Conductive Type		Semi-insulated	

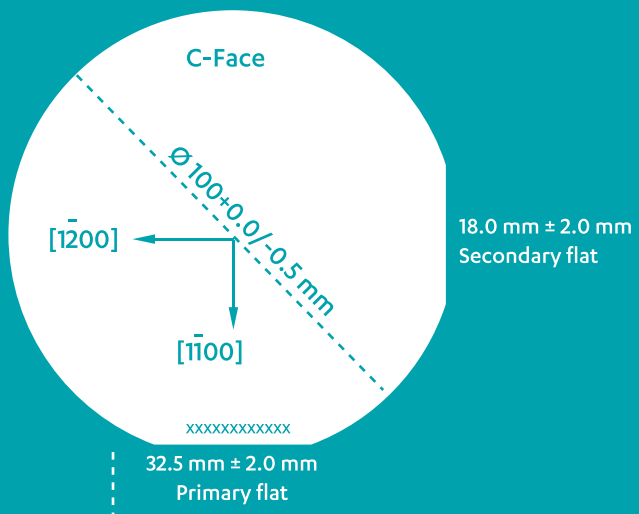
PROPERTIES, TERMINOLOGY, AND METHODS

01 Diameter /Primary Flat/Laser-mark information shown as Figure 5

Figure 5



A laser mark of 12 characters consist of numbers and letters starts above the Notch flat, with the depth of 60-70μm and length of 16.5mm



A laser mark of 12 characters consist of numbers and letters starts above the primary flat, with the depth of 60-70μm and length of 16.5mm

Semi-insulating SiC Substrate

CRYSTAL QUALITY SPECIFICATIONS

Item	4Inch	6Inch
Resistivity	≥1E9Ω•cm	
Polytype	None permitted	
Micropipe Density	≤0.3/cm²	≤0.5/cm²
Hex Plates by high intensity light	None permitted	
Conductive Type	Semi-insulated	
Visual Carbon Inclusions by high intensity light	Cumulative area ≤0.05%	

PROPERTIES, TERMINOLOGY, AND METHODS

01 Resistivity

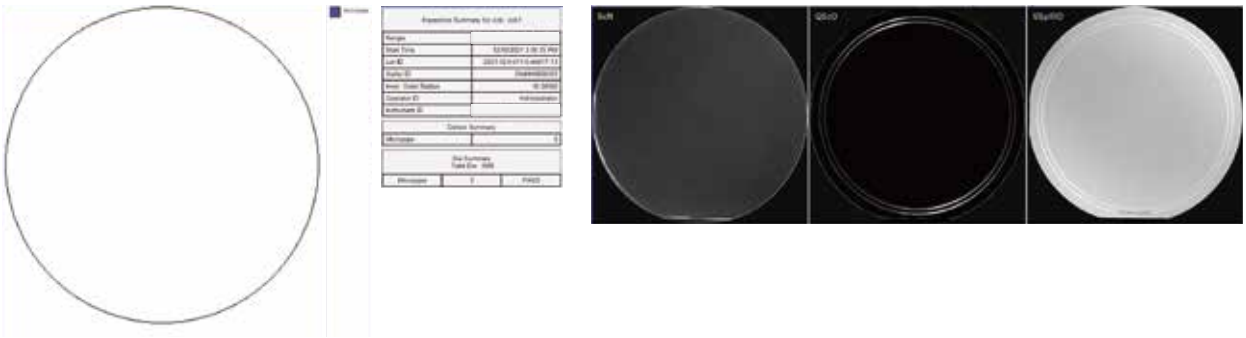
Tested by Non-contact sheet resistance

Figure 6

The resistivity of 04/07/11th wafer in 0001 direction is greater than the detection limit

02 Micropipe density

Figure 7



n-Type & Semi-insulating
WAFERING SPECIFICATIONS

* n-Pm=n-Type Pm-Grade n-Ps=n-Type Ps-Grade SI=Semi-insulating

Item	6Inch			4Inch
	n-Pm	n-Ps	SI	SI
TTV(GBIR)[1]	≤6μm			
BOW(GF3YFCD)-Absolute Value[1]	≤15μm	≤25μm		≤15μm
Warp(GF3YFER)[1,2]	≤25μm	≤40μm		≤25μm
LTV(SBIR)- 10mm x 10mm	≤2μm			
Wafer Edge[3]	Bevelling			

PROPERTIES, TERMINOLOGY, AND METHODS

01 TTV/Bow/Warp

Mapping data can be provided if required

02 Warp

The substrate is placed horizontally in the instrument during testing

03 Wafer edge

R (C)-Type is our standard bevelling process, and T-type bevelling can also be provided

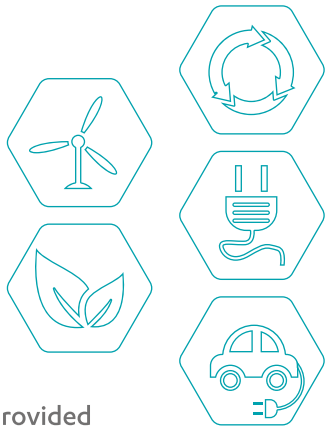
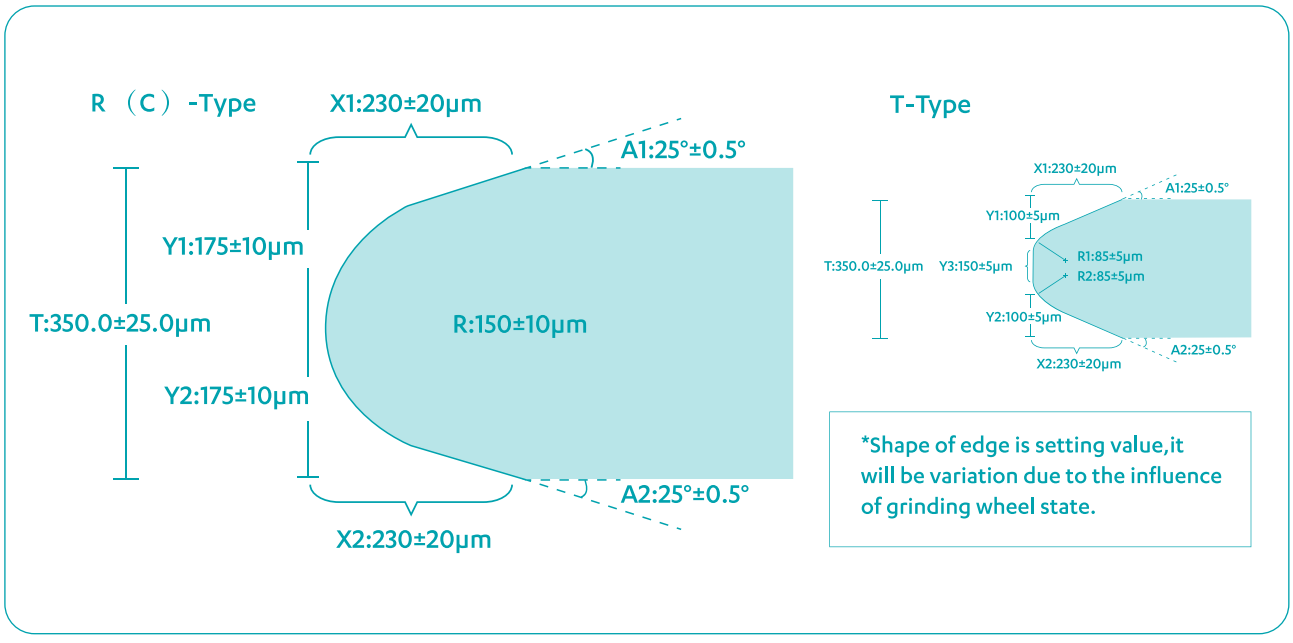


Figure 8

The figure below shows the bevelling of 350μm products. And please contact us for the bevelling of 500μm products



n-Type & Semi-insulating
SURFACE FINISH

* n-Pm=n-Type Pm-Grade n-Ps=n-Type Ps-Grade SI=Semi-insulating

Item	6Inch			4Inch
	n-Pm	n-Ps	SI	SI
Surface Finish	Double side Optical Polish,Si Face CMP			
Surface Roughness[1]	（10μm x 10μm） Si-Face Ra≤0.2nm C-Face Ra≤0.5nm		（5μm x 5μm） Si-Face Ra≤0.2nm C-Face Ra≤0.5nm	
Edge Chips[2]	None Permitted （length and width≥0.5mm）			
Indents[2]	None Permitted			
Scratches[3]（Si-Face）	Qty.≤5 Cumulative length≤0.5×wafer diameter			
Cracks[4]	None Permitted			
Edge Exclusion	3mm			

PROPERTIES, TERMINOLOGY, AND METHODS

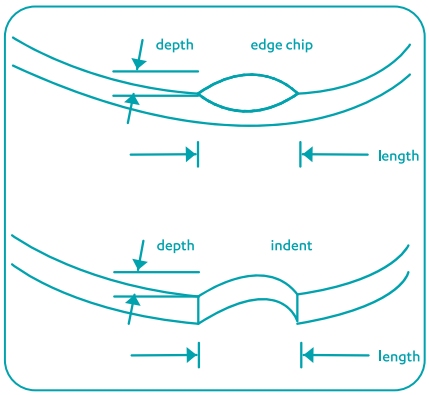
01 Surface Roughness

Every substrate is tested by Atomic Force Microscopy

02 Edge chips / Indents

Any edge anomaly saw exit marks conforming to the definition and greater than 0.25mm （*In SiC materials, 0.5 is usually used） in radial depth and peripheral length shown as Figure 9, (* Reference SEMI M55) every substrate is inspected by diffuse lighting

Figure 9



03 Scratch

Any anomaly conforming to the definition and having a length-to-width ratio greater than 5:1 and visible under intense illumination (* Reference SEMI M55)

04 Crack

Any anomaly conforming to the definition and greater than 0.25mm in total length (* Reference SEMI M55) (*No visible cracks are allowed in our standards)

Packaging

Cassette	Multichip cassette : 25 pcs per cassette
	Single cassette : 1 pc per cassette
Package	Multichip Cassette :
	-Inner: vacuum sealed plastic bag
	-Outer: vacuum sealed aluminized plastic bag
	Single Cassette:
	-Inner: sealed plastic bag without vacuum
	-Outer: sealed aluminized plastic bag without vacuum
Box & Carrier	Paper box filled with foam
Label	Label on the cassette & outer package shows the Wafer No.& Lot No.& Quantity
	-No label on the inner package

*We also offer Dummy products, the following parameters are different with P-Grade product.

* SI=Semi-insulating

	6Inch		4Inch
Property	n-Type	SI	SI
Polytype	Cumulative area≤5%		
Micropipe density	≤5/cm²		
Hex Plates by high intensity light	Cumulative area≤5%		
Resistivity	0.014-0.028 Ω·cm	≥1E5 Ω•cm	
Visual Carbon Inclusions	N/A		
Dislocation density	N/A		
TTV(GBIR)	≤10μm		
Bow (GF3YFCD)- Absolute value	≤40μm		≤30μm
Warp (GF3YFER)	≤60μm		≤45μm
LTV (SBIR)-Max ,10mm x 10 mm	≤3μm		
Edge chips	Qty.2 ≤1.0 mm width and depth		
Scratches （Si-face）	Qty.5 Cumulative length≤1.5×wafer diameter		

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